Input

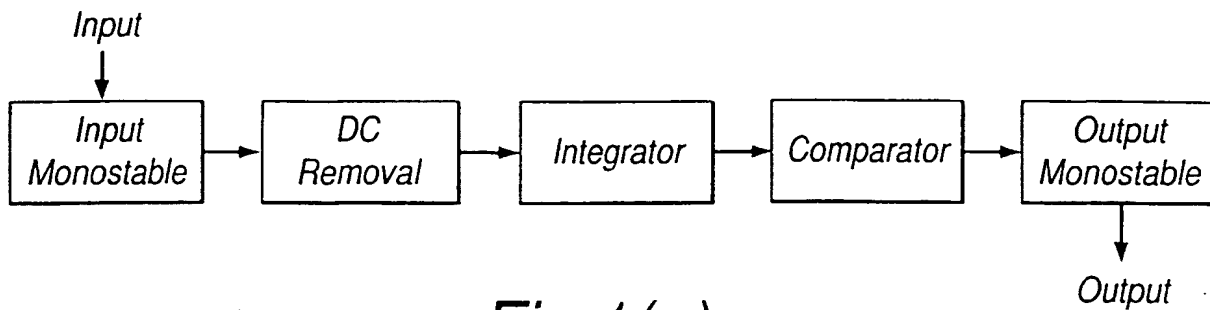| Input Monostable | → | DC Removal | → | Integrator | → | Comparator | → | Output Monostable |

Output

Fig.1(a)

Jitter

Fig.1(b)

op2

op3

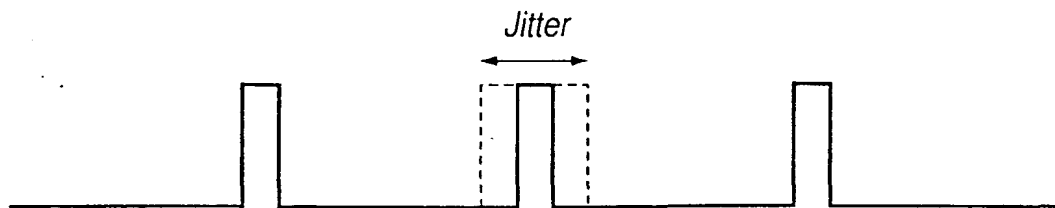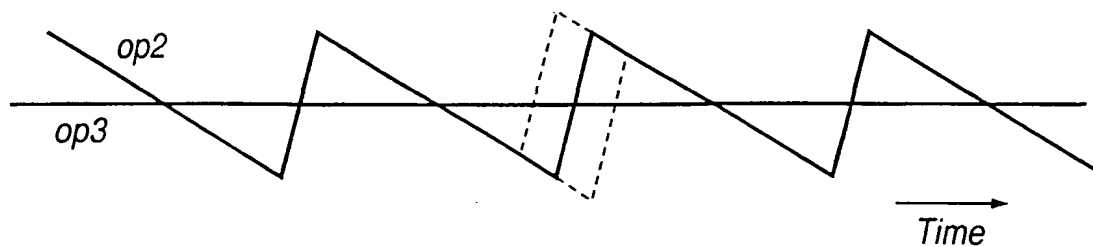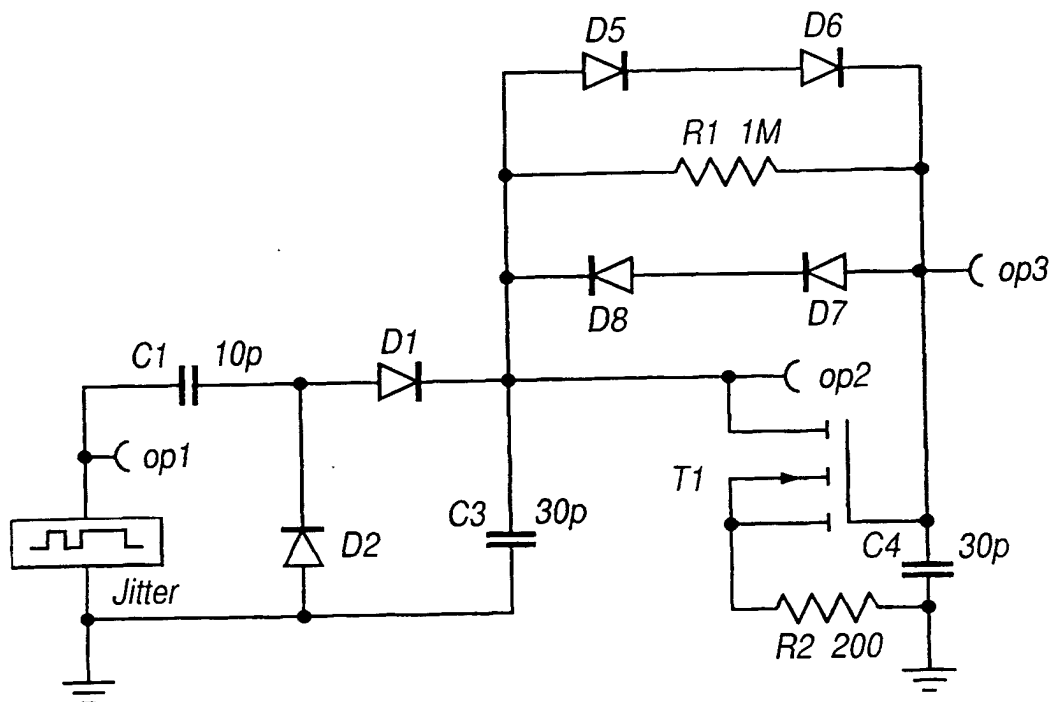Time

Fig.1(c)

Fig.1 Anti Jitter Circuit Principle:-

(a) Basic Block Diagram
(b) Input with jitter on central pulse
(c) Integrator output (op2) and Comparator switching level (op3)

D5   D6

R1 1M

D8   D7   op3

C1 10p   D1   op2

op1

Jitter   D2   C3 30p   T1   C4 30p

R2 200

T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4usec at 1/3 rate

Fig.2(a)
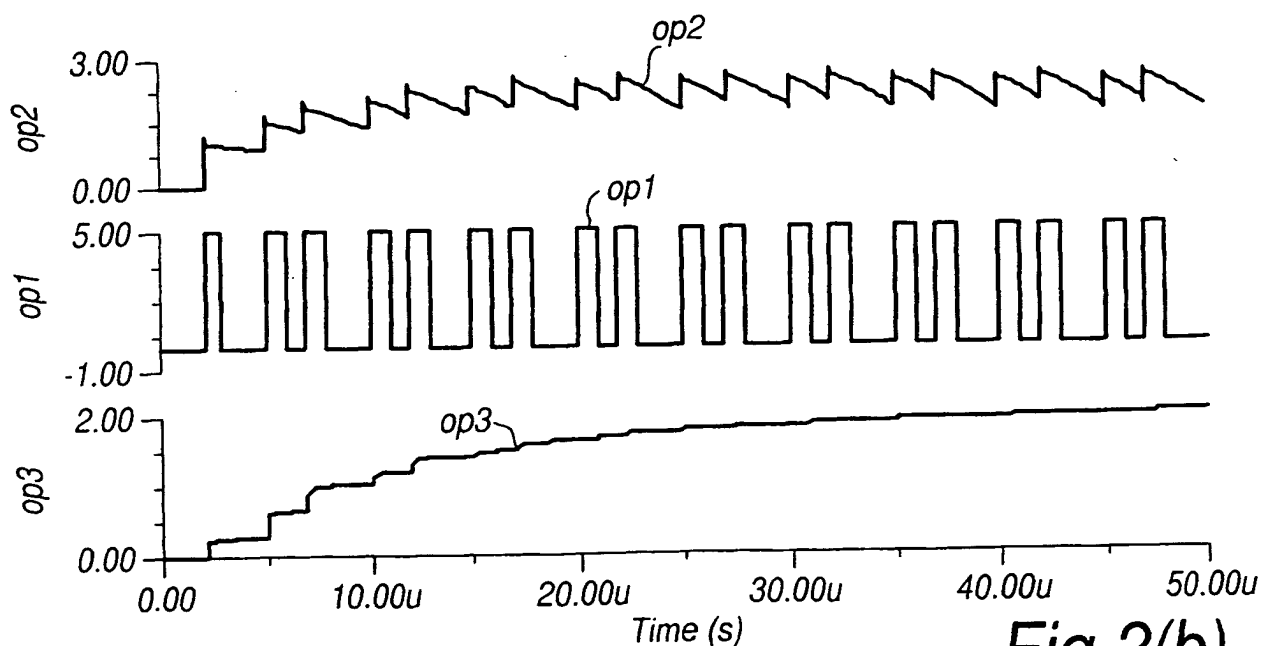
Fig.2(b)

Fig.2(c)

Fig.2(d)

D5   D6

R1   10M

D8   D7

op3

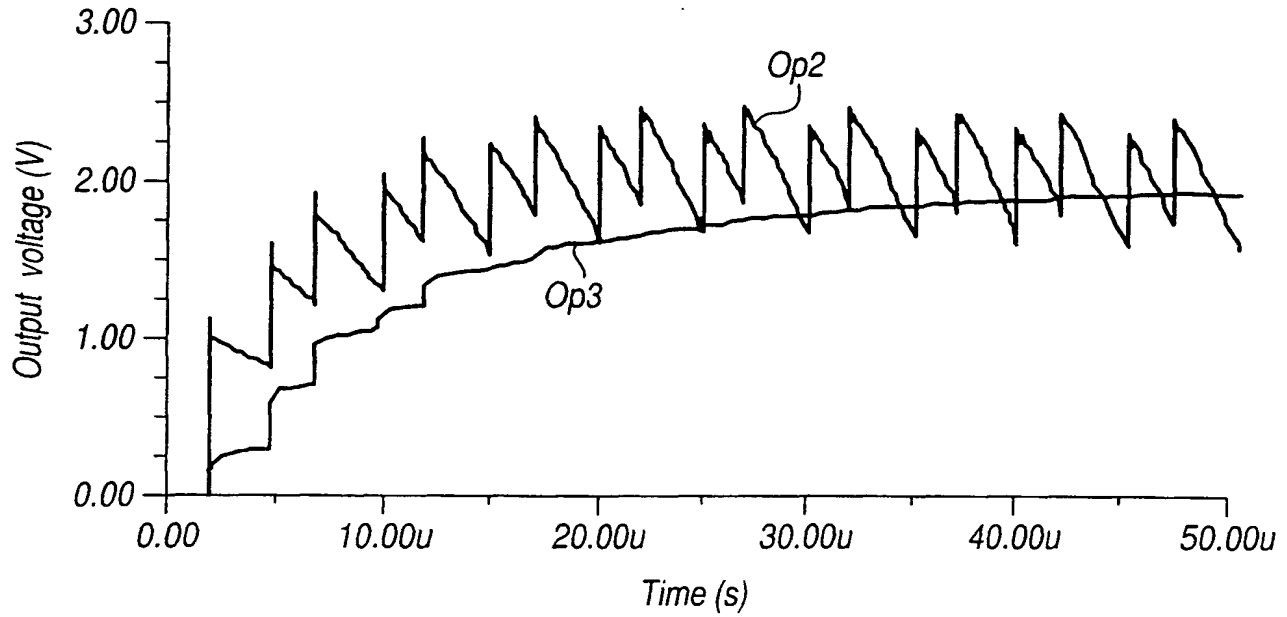Input 10KHz   D1
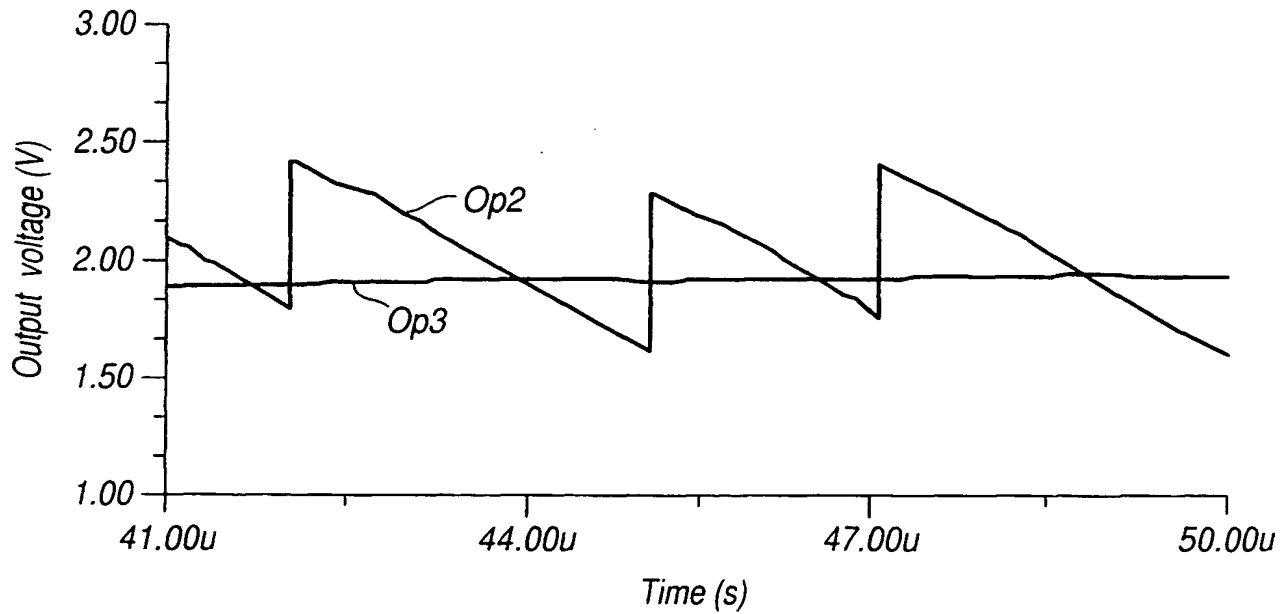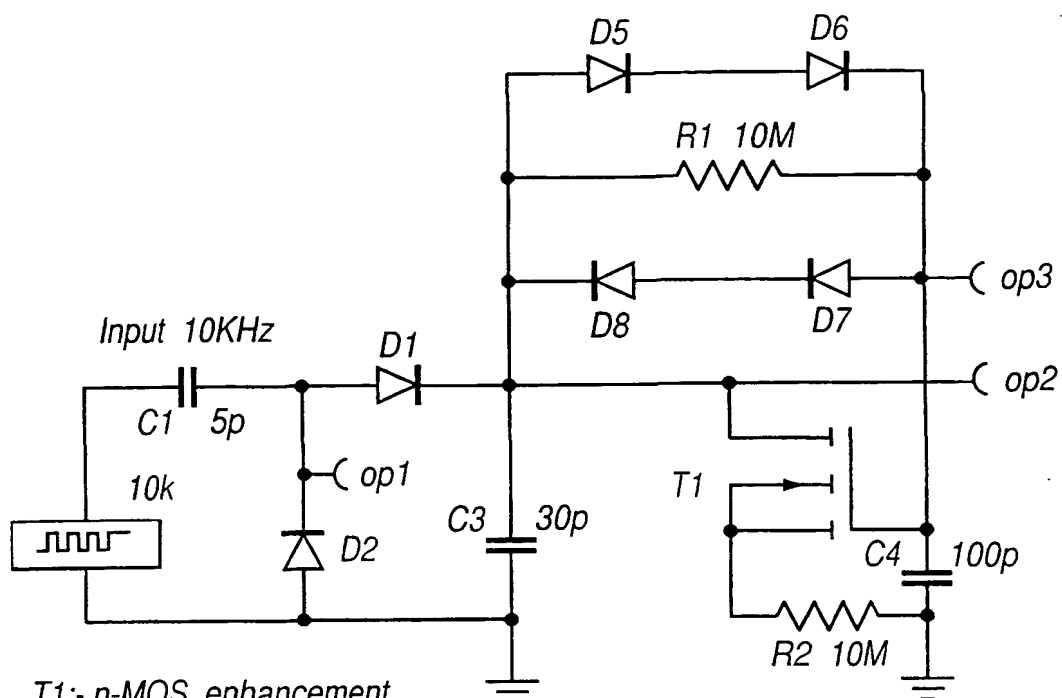
op2

C1   5p

op1

10k

C3   30p

D2

T1

C4   100p

R2   10M
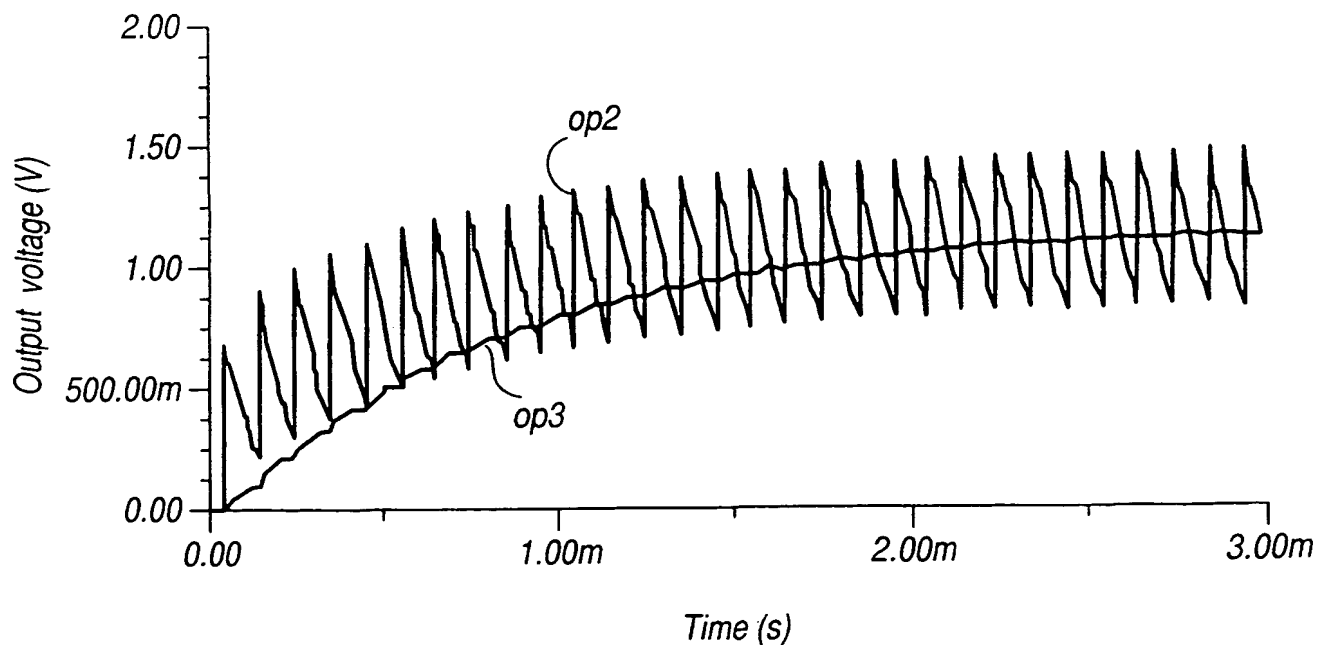
T1:- n-MOS enhancement
Threshold 0v   Beta 300uA/VV

op2 and op3 to differential comparator

Fig.3(a)

op2

op3

2.00

1.50

1.00

Output voltage (V)

500.00m

0.00

0.00   1.00m   2.00m   3.00m

Time (s)

Fig.3(b)

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Input 50MHz

C1 5p

50M

op1

D2

D1

D5   D6

R1 50k

D8   D7

op3

op2

T1

C3 30p

C4 10p

R2 100
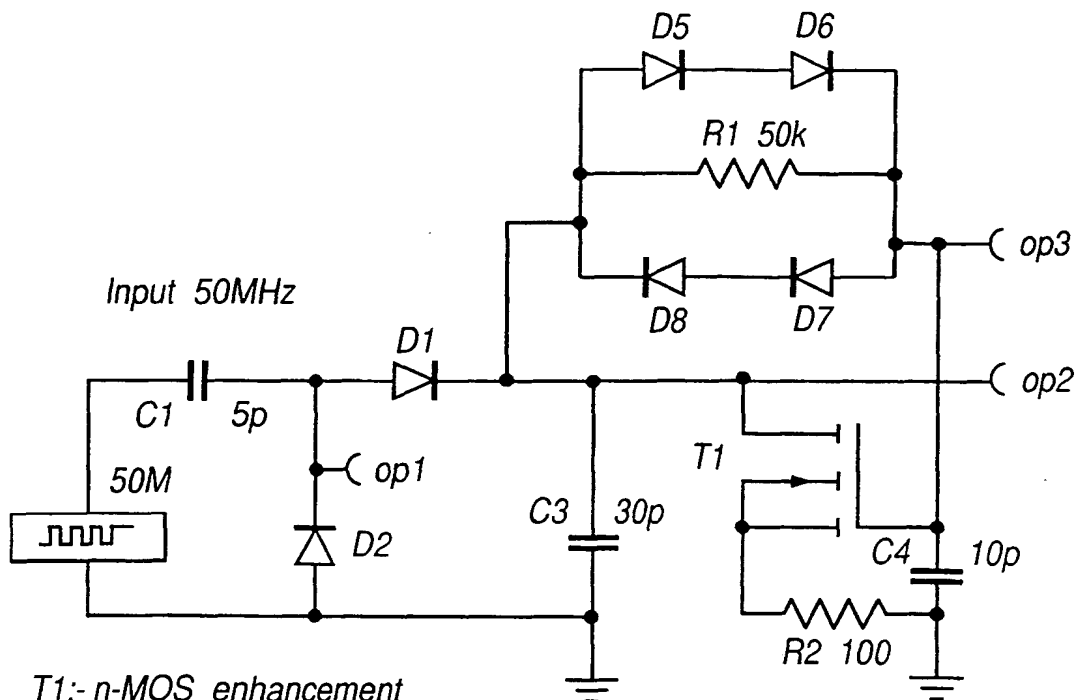
T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig.4(a)

Fig.4(b)

D5   D6

R1 10k

op3

D8   D7

Input 5GHz

op2

D1

C1 0.1p

5G

op1

T1

C4 0.1p

D2

C3 0.5p

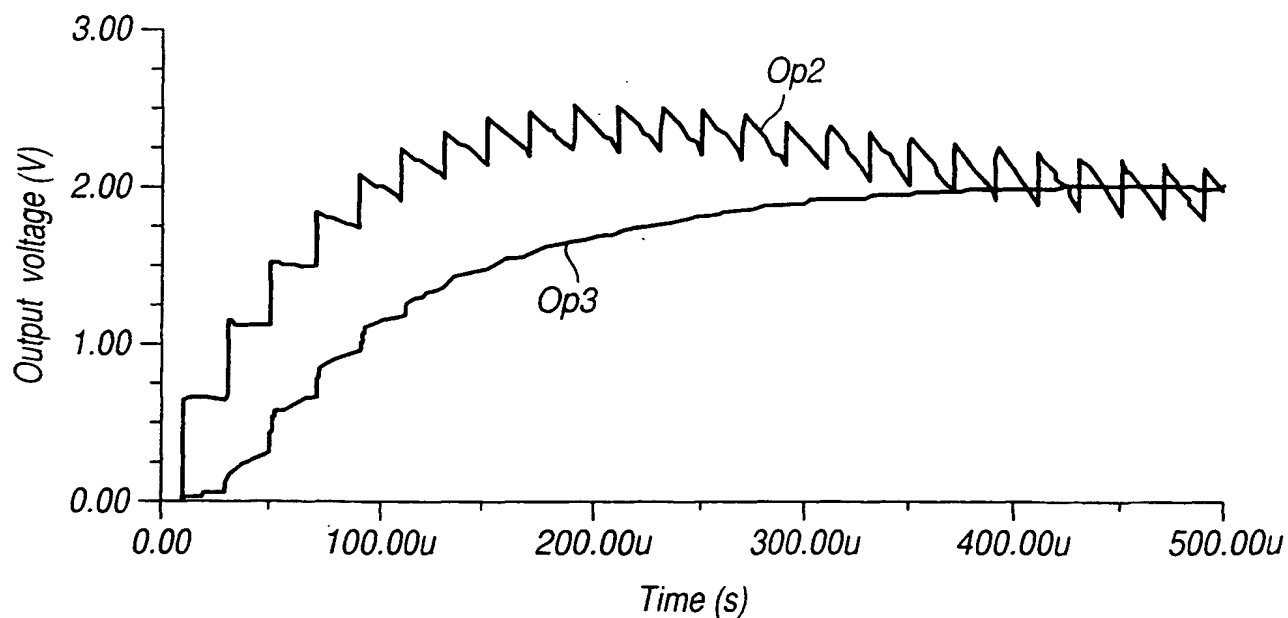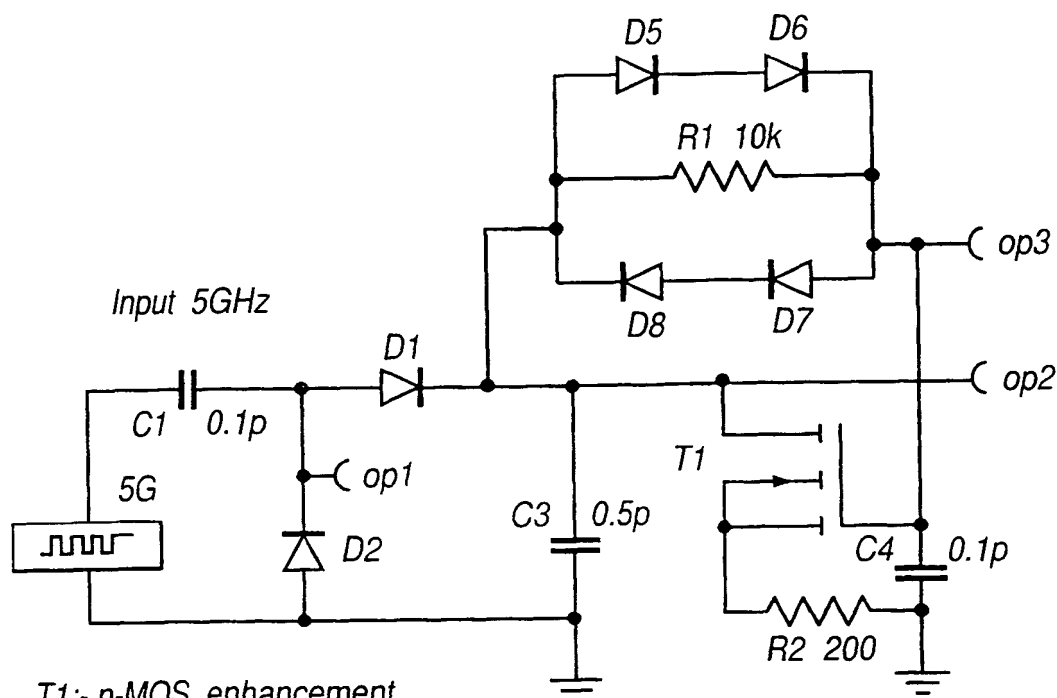R2 200

T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig.5(a)

Fig.5(b)
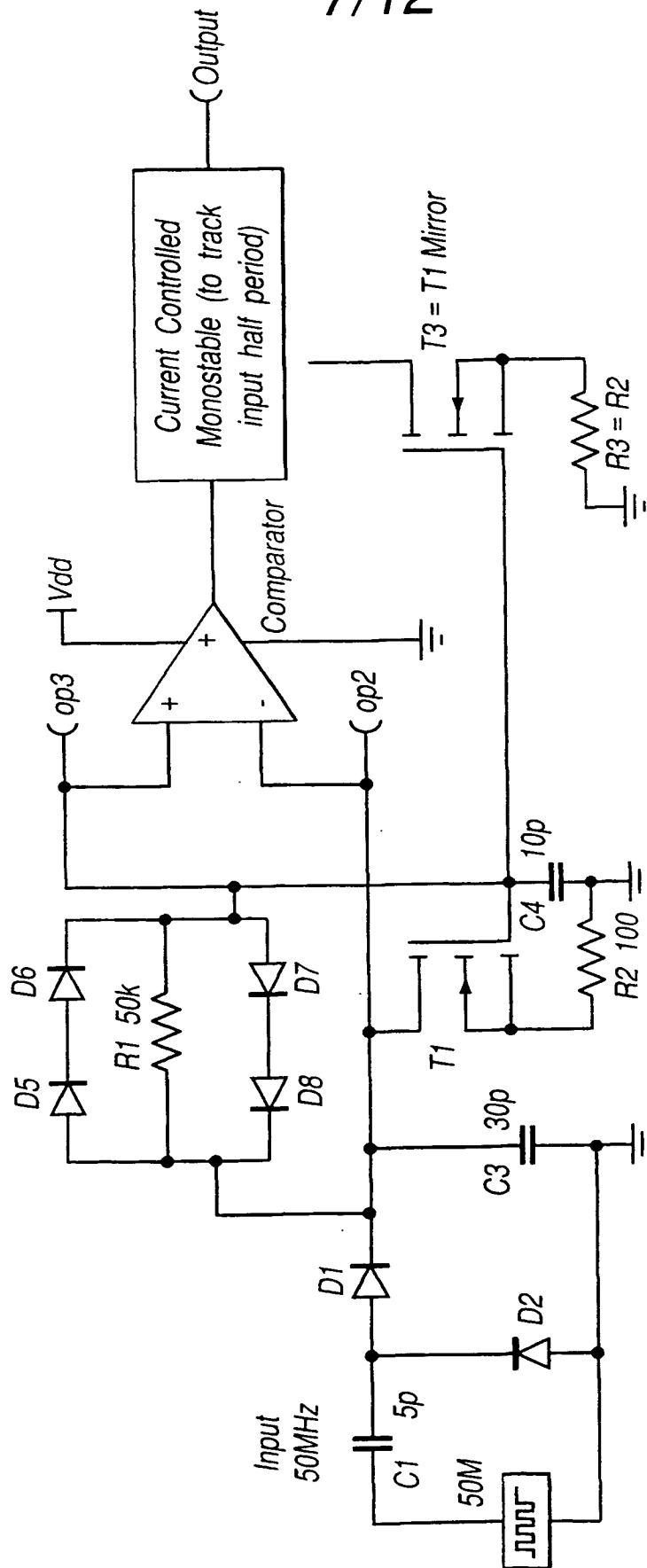
Fig.6

AAJC with Comparator and input-tracking Output Monostable
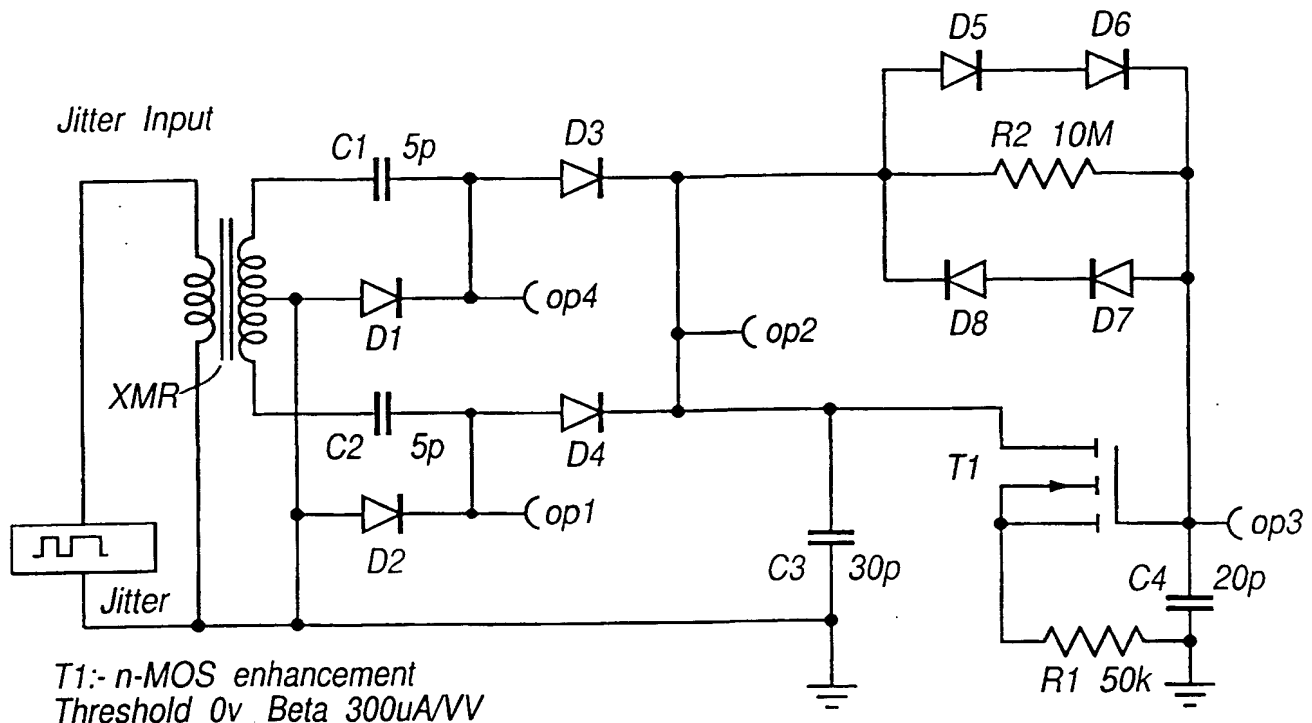
T1:-n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Jitter Input

T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

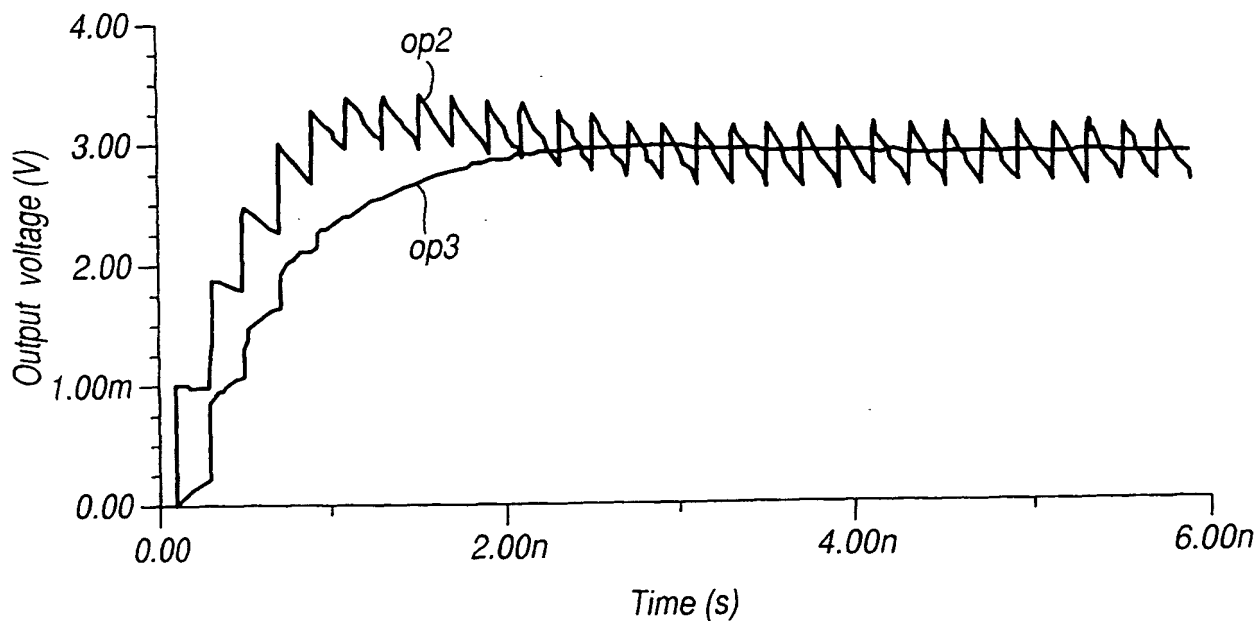Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
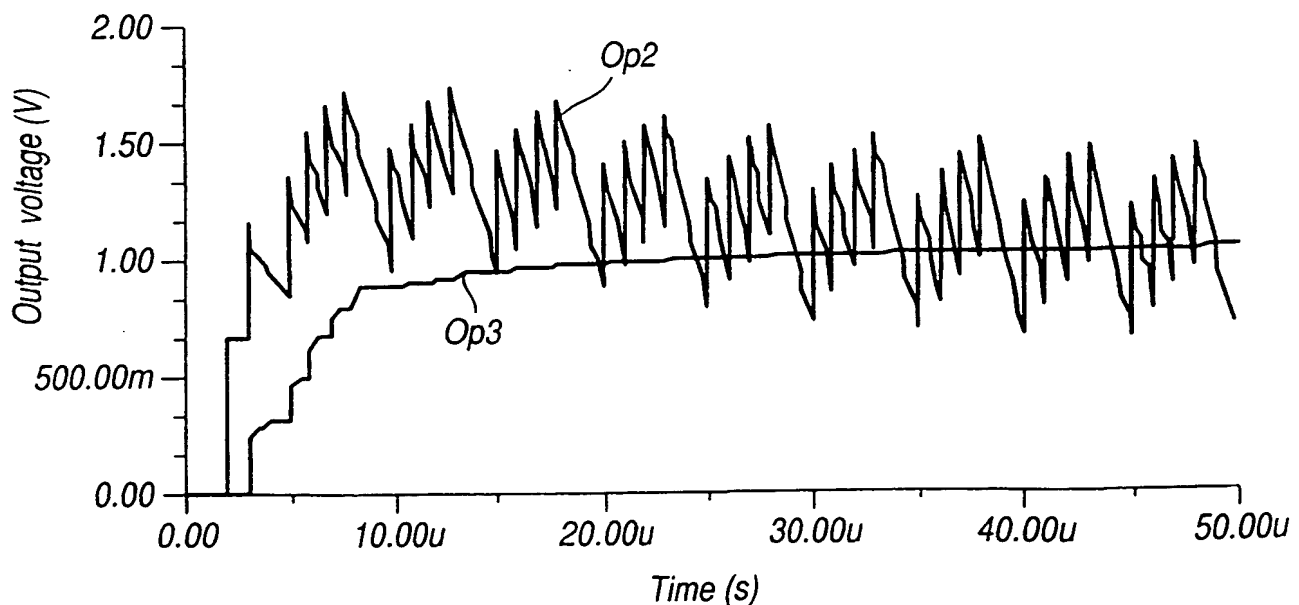= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.7(a)

Fig.7(b)

Fig.7(c)

T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
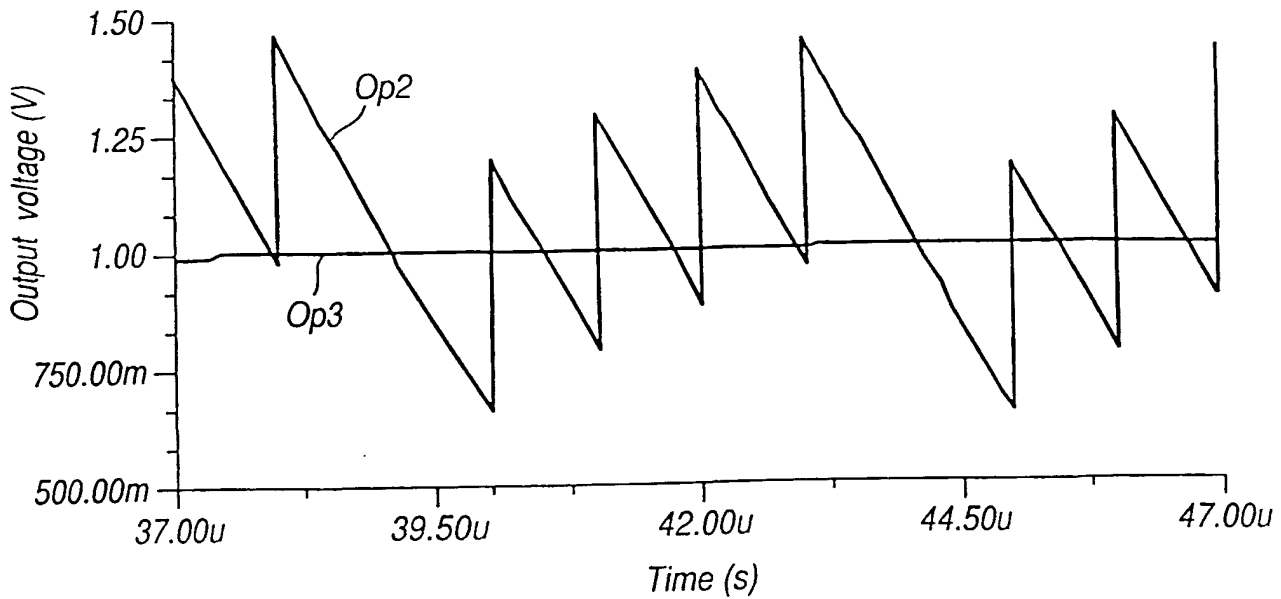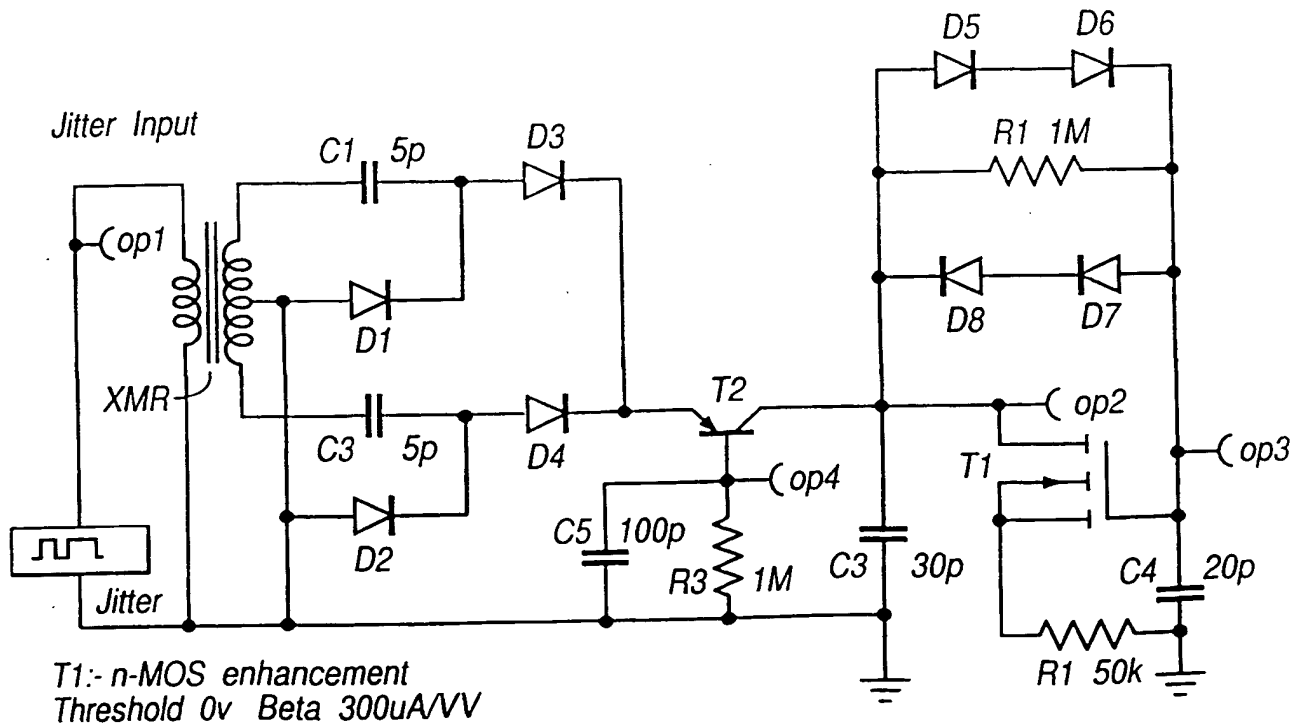= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.8(a)

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Fig.8(b)

Fig.8(c)

T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 300 degrees
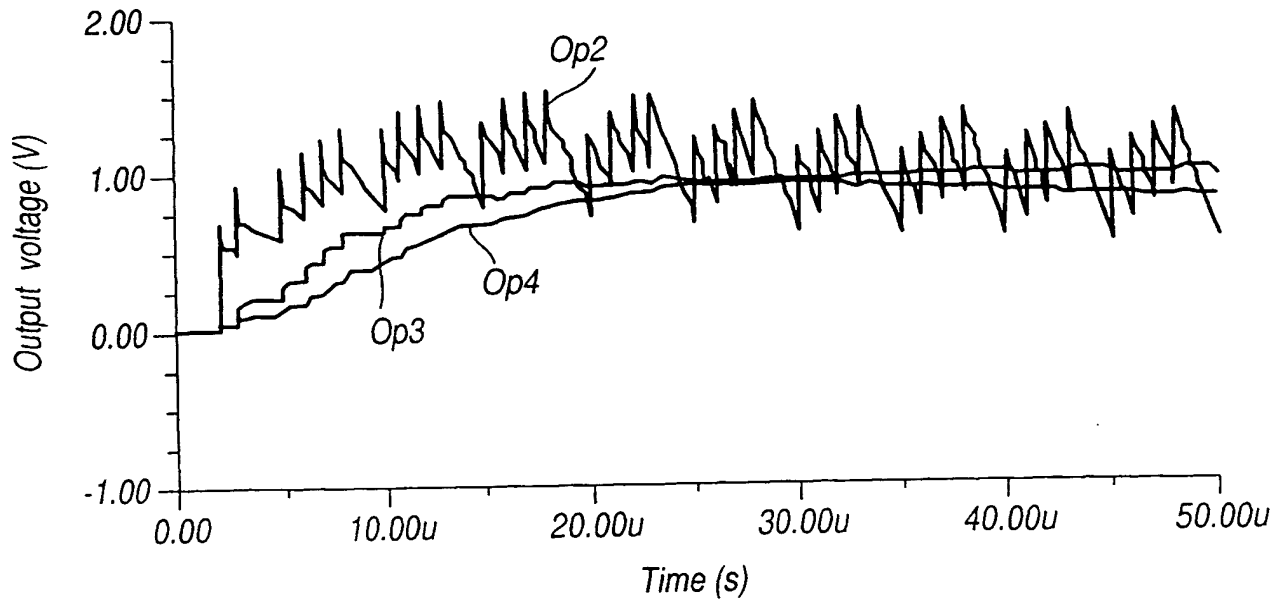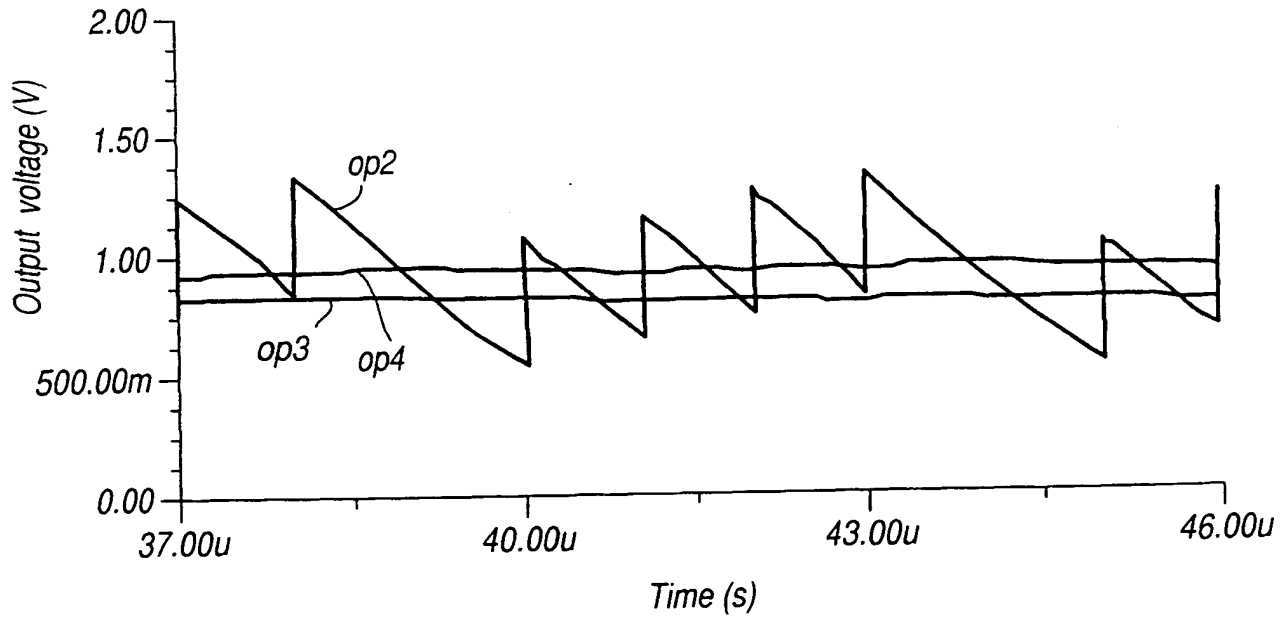= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.9(a)

Fig.9(b)

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Fig.9(c)

Fig.10